Notice of Allowability	Application No.	Applicant(s)	
	10/707,874	CHANG, KENT KUOHUA	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Examiner's Amendment agreed to by Applicant's representative*.

2. ☒ The allowed claim(s) is/are *8,9 and 11-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 20060412
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060427* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 February 2006 has been entered.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ms. Belinda Lee on 27 April 2006.

The application has been amended as follows:

In the specification in paragraph 0001, after 10/248,374 insert --now U. S. Patent 6,720,613--.

In the claims:

8. (currently amended) A method of fabricating a multi-bit flash memory, comprising:

providing a substrate;

forming a tunneling oxide layer on the substrate;

forming a conductive layer on the tunneling oxide layer;

forming an isolation layer in the conductive layer to partition the conductive layer into more than two conductive blocks arranged in an array with a plurality of rows extending from a region predetermined for forming one bit line to another region predetermined for forming another bit line and a plurality of columns, wherein each row comprises tow conductive blocks, and each column comprises more than two conductive blocks, wherein the step of forming the isolation region further comprises:

forming a patterned photoresist layer on the conductive layer to expose a part of the conductive layer predetermined for forming the isolation region;

performing an ion implantation step to implant dopant into the exposed conductive layer; and performing an annealing process to react the dopant with the silicon of the conductive layer to form the isolation region;

forming a gate dielectric layer on the conductive layer;

patterning the gate dielectric layer and the conductive layer to form a floating gate comprising a predetermined number of conductive blocks arranged in an array having pluralities of rows and columns, wherein each row comprises a plurality of conductive blocks and each column comprises a plurality of conductive blocks, and wherein the patterned gate dielectric layer is formed vertically above the predetermined number of blocks arranged in the array;

forming the bit lines in the substrate at two sides of the floating gate;

forming a control gate on the floating gate so that each multi-bit cell of the multi-bit flash memory comprises said control gate, said patterned gate dielectric layer and said floating gate comprising said plurality of conductive blocks arranged in said array; and

performing a step of threshold voltage adjustment to result in different threshold voltages of the channel regions under the conductive blocks of different rows.

10. (cancelled)

11. (currently amended) The method according to Claim ~~10~~ 8, wherein the dopant includes oxygen ions.

14. (currently amended) The method according to Claim ~~10~~ 8, wherein the dopant includes nitrogen ions.

15. (currently amended) The method according to Claim ~~10~~ 8, wherein the annealing process is performed at about 950°C to about 1150°C.

3. Claims 8, 9 and 11 – 20 are allowed over the prior art of record.

4. The following is an examiner's statement of reasons for allowance: Wu in the United States Patent Application Publication US 2003/0193064 A1 and related text, discloses most of the claimed invention. However, Wu does not disclose, teach or suggest forming a patterned photoresist layer on the conductive layer to expose a part of the conductive layer predetermined for forming the isolation region; performing an ion implantation step to implant dopant into the exposed conductive layer; and performing an annealing process to react the dopant with the silicon of the conductive layer to form the isolation region. Wu, on the other hand, discloses etching part of the conductive film to form a trench, oxidizing the sidewalls of the remaining

conductive film, depositing another conductive film in the trench and then patterning the conductive film to form the conductive columns and rows. It would destroy the reference of Wu if it were modified to read on the claimed invention. Therefore the claimed invention as a whole is neither anticipated nor rendered obvious over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Fri 12pm-7:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fernando L. Toledo
Patent Examiner
Art Unit 2823

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27 April 2006